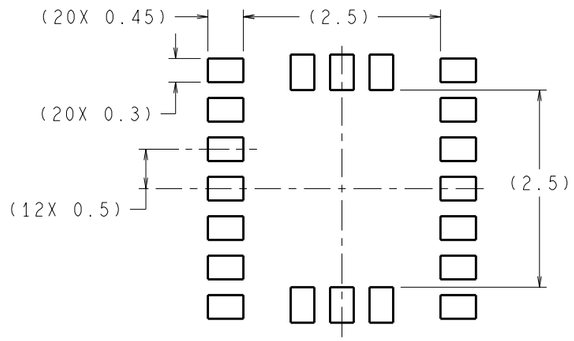
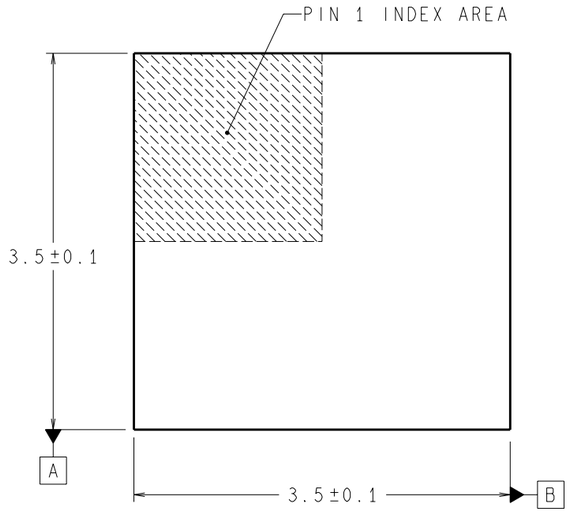
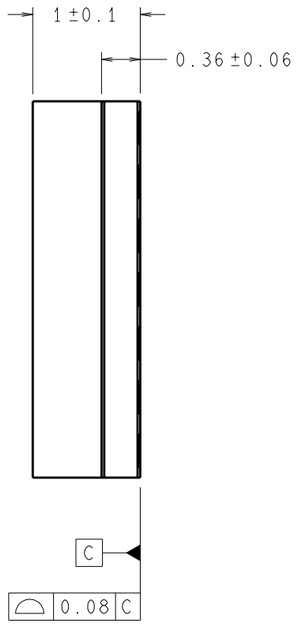
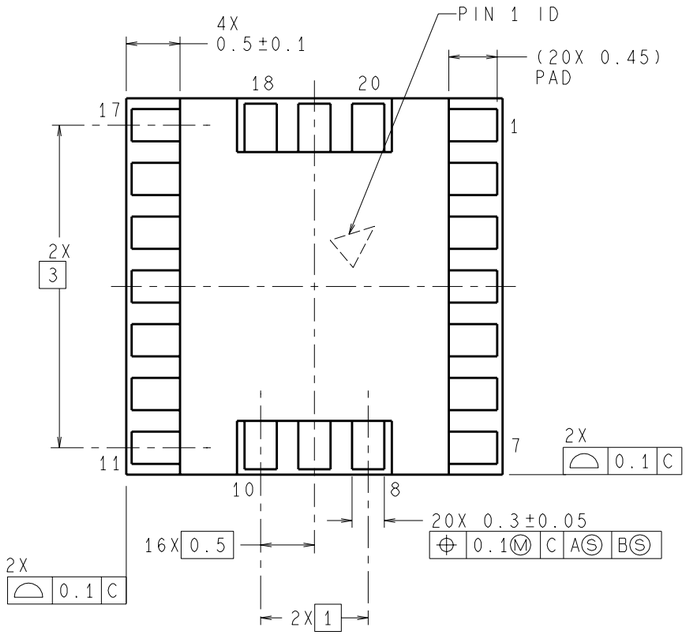
REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	12419	03/07/2000	TL/TF



RECOMMENDED LAND PATTERN
1:1 RATIO WITH PACKAGE SOLDER PADS







DIMENSIONS ARE IN MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

1. MATERIAL: BT RESIN CCL-HL832 WITH TAIYO PSR4000 AUS5 SOLDER MASK.
2. PLATING: Cu 15 TO 20 MICROMETERS
   Ni 10 ± 5 MICROMETERS
   Au 1 ± 0.5 MICROMETER
3. REFERENCE JEDEC REGISTRATION MO-208, VARIATION CCEA-1, DATED DECEMBER 1999.

APPROVALS	DATE
DRAWN T. LEQUANG	03/06/2000
DFTG. CHK. MARTA SUCHY	03/07/2000
ENGR. CHK. TONYA FRIDLYAND	03/07/2000

PROJECTION
INCH [MM]

National Semiconductor
2900 Semiconductor Dr, Santa Clara, CA 95052-8090

CSP, PLASTIC, LAMINATED, 3.5 X 3.5 X 1.0 mm BODY, 20 L, 0.5 mm PITCH

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-SLB20B	A

FORMERLY: N/A

SHEET 1 of 1